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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,158	01/22/2002	Tsutomu Nakamura	020062	7925
38834	7590	02/08/2006	EXAMINER	
WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP 1250 CONNECTICUT AVENUE, NW SUITE 700 WASHINGTON, DC 20036			SELBY, GEVELL V	
		ART UNIT	PAPER NUMBER	
			2615	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/051,158	NAKAMURA ET AL.	
	Examiner Gevell Selby	Art Unit 2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 14 November 2005.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 3,6 and 13-15 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) 14 is/are allowed.  
 6) Claim(s) 3,6,13 and 14 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 22 January 2002 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                    | Paper No(s)/Mail Date. _____.   |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|   | 6) <input type="checkbox"/> Other: _____.                                   |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments with respect to claims 3, 6, 13, and 15 have been considered but are moot in view of the new ground(s) of rejection.
2. Applicant's arguments, see the response, filed 11/14/05, with respect to the claim 14 have been fully considered and are persuasive. The 35 U.S.C. 103(a) rejection of claim 14 has been withdrawn.

### ***Specification***

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 3, 6, 13, and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakamura, US 6,472,761.**

In regard to claim 3, Nakamura, US 6,472,761, discloses a solid-state image pickup apparatus comprising:

a solid-state image pickup device chip (see figure 1b, elements 20 and 32) having a bump (see figure 1b, elements 21 and 22) formed thereon, and a hermetic seal portion provided over the solid-state image pickup device chip having a flat-plate portion (see figure 1b, element 10) formed of a transparent member (see column 7, lines 54-60) and a frame portion disposed on a side portion of a lower surface of the flat-plate portion (see figure 6, element 32); edge sides of said solid-state image pickup device chip and those of said hermetic seal portion being substantially coincident with each other (see figure 1b; the hermetical seal portion formed by the transparent substrate 10 and the frame portion of the solid state device 32 are substantially coincident with each other)

said frame portion at least including a metal wiring (see figure 6, elements 13), a bump (see figure 1b, element 21) formed on said solid-state image pickup device chip and electrically connected to the metal wiring (see figure 1b and column 7, lines 51-53 and column 7, lines 61+), and a sealed region for sealing the periphery of the bump by a sealing material (see figure 1b, element 40, column 7, lines 54-59);

wherein the frame portion further includes a frame base portion (see figure 1b, element 44) and said metal wiring is formed on one surface of said frame base portion (wiring 13 is formed on a side surface) while the other surface of the frame base portion is adhered to said flat-plate portion (transparent substrate 10 is formed on the top surface).

In regard to claim 13, Nakada, US 6,399,995, discloses the solid-state image pickup apparatus comprising:

a solid-state image pickup device chip (see figure 1b, elements 20 and 32);

and

a hermetic seal portion comprising a flat-plate portion (see figure 1b, element 10) formed of a transparent member (see column 7, lines 54-60) provided over the solid state image pickup device chip and a frame portion (see figure 6, element 32) at least including a metal wiring (see figure 6, elements 13) disposed on a side portion of a lower surface of the flat-plate portion, a bump (see figure 1b, elements 21 and 22) formed on said solid-state image pickup device chip and electrically connected to the metal wiring (see figure 1b and column 7, lines 51-53 and column 7, lines 61+), and a sealed region for sealing the periphery of the bump by a sealing material (see figure 1b, element 40, column 7, lines 54-59);

edge sides of said solid-state image pickup device chip and those of said hermetic seal portion being substantially coincident with each other (see figure 1b: the hermetical seal portion formed by the transparent substrate 10 and the frame portion of the solid state device 32 are substantially coincident with each other)

wherein a wiring region (figure 8b, element 33) is formed from an electrode pad (see figure 1b, element 14) provided on said solid-state image pickup device chip to a side surface so that an external terminal can be electrically

connected to the wiring region or the electrode pad region (see column 8, lines 5-12).

In regard to claims 6 and 15, Nakamura, US 6,472,761, discloses the solid-state image pickup apparatus according to claims 3 and 13, respectively, wherein an anisotropic conductive material is used as said sealing material (see column 14, lines 30-34).

*Allowable Subject Matter*

6. Claim 14 is allowed.
7. The following is a statement of reasons for the indication of allowable subject matter:

In regard to claim 14, the prior art does not disclose a fabricating method of solid-state image pickup apparatus with the combination of limitations claimed for the invention, specifically the limitations of:

over an entire wafer having a large number of solid-state image pickup device chips formed thereon, integrally and at once in a manner corresponding to each individual solid-state image pickup device chip, forming a hermetic seal portion comprising a flat-plate portion made of a transparent member, and a frame portion at least including a metal wiring disposed at a side portion of a lower surface of the flat-plate portion having a metal wiring, a bump formed on solid-state image pickup device chip and electrically connected to the metal wiring, and a seal region for sealing the periphery of the bump by a sealing material so that the frame portion is disposed on the lower surface of the flat-

plate portion where a transparent member extended over the entire wafer is used as the flat-plate portion; and

separating the wafer having the integrally formed hermetic seal portions thereon into solid-state image pickup device chips each having an individual hermetic seal portion, as claimed in claim 14.

*Conclusion*

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ono, US 6,774,481, discloses a solid-state pickup device with a bump on the image pickup device chip.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Art Unit: 2615

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gevell Selby whose telephone number is 571-272-7369. The examiner can normally be reached on 8:00 A.M. - 5:30 PM (every other Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on 571-272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gvs



DAVID OMETZ  
SUPERVISORY PATENT EXAMINER